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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,508	12/04/2003	Wiley Eugene Hill	H1415	7175

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,508	HILL ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *11 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03 & 03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 12/04/2003 is acceptable.

Claim Objections

2. Claims 11 and 20 are objected to because they contain typographical errors:

- **Claim 11**, line 1, recites:

"device of claim 11"

which should be:

"device of claim **10**"

- **Claim 20**, line 2, recites:

"functions a drain region"

which should be:

"functions **as** a drain region"

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1, 5, and 16-18** are rejected under 35 U.S.C. 102(e) as being anticipated by Cleeves et al. U.S. Patent 6,580,124.

Cleeves discloses in Figures 1 and 2 and respective portions of the specification a memory device as claimed.

Referring to independent **claim 1**, Cleeves discloses a memory device, comprising:

a first conductive layer (104, Fig. 1a), wherein a portion of the first conductive layer acts as a source region (column 2, lines 15-20) for the memory device;

a conductive structure (102) formed on the first conductive layer, the conductive structure having a first end and a second end opposite the first end, wherein the first end is disposed adjacent the portion of the first conductive layer that acts as the source region for the memory device and wherein the second end acts as a drain region (108, column 2, lines 15-20) for the memory device;

a plurality of dielectric layers (114-117, Fig. 1b) formed around at least a portion of the conductive structure, wherein at least one of the dielectric layers acts as a floating gate electrode for the memory device (column 2, lines 50-65); and

a control gate (120) formed over the plurality of dielectric layers.

Note that "over" is interpreted broadly.

Referring to independent **claim 16**, and using the same reference characters and citations as detailed above where applicable, Cleeves discloses a non-volatile memory array, comprising:

a first conductive layer (202, Fig. 2q) formed on a substrate, wherein portions of the first conductive layer act as source regions for memory cells in the memory array;

a plurality of structures (233, Figs. 2p-2r) formed on the first conductive layer, wherein each of the plurality of structures functions as a channel region for one of the memory cells;

a plurality of dielectric layers (218/234, fig. 2r) formed around portions of each of the plurality of structures, wherein at least one of the plurality of dielectric layers functions as a charge storage electrode for one of the memory cells; and

at least one conductive layer (224 or 236) formed over the plurality of dielectric layers for each of the memory cells.

Note again that "over" is interpreted broadly. Note also that Figures 2's is a method for fabricating the device of figures 1's (column 5, lines 50+), therefore, respective reference characters will be used where it is best disclosed, although the respective reference characters actually pertain to all the figures.

Referring to **claims 5 and 17**, Cleeves further discloses that the plurality of dielectric layers comprises:

a first oxide layer formed around the conductive structure,

a nitride layer formed around the first oxide layer, and

a second oxide layer formed around the nitride layer, wherein the nitride layer functions as the charge storage electrode or as the floating gate electrode (ONO, column 2, lines 50-65).

Referring to **claim 18**, Cleeves further discloses a plurality of bitlines (230, Fig. 2q), wherein each of the plurality of bitlines contacts a number of the plurality of structures ("pillars", column 9, lines 8-11).

4. **Claims 10 and 12-13** are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. U.S. Patent Application Publication 2002/0028541.

Lee discloses in Figures 1A, 1B, and 7 and respective portions of the specification a memory device as claimed.

Referring to independent **claim 10**, Lee discloses a memory device, comprising:

a substrate (101 in Fig.1A but not shown in Fig. 7);

a first insulating layer formed on the substrate (not shown in these figures);

a conductive structure (104/106, Fig. 1A or 206/208, Fig. 7) formed over the first insulating layer, the conductive structure functioning as a channel region for the memory device (paragraphs [0123] and [0128]);

a plurality of dielectric layers (704/706/708, Fig. 7) formed around (best seen in Fig. 1B and explained in paragraph [0125]) at least a portion of the conductive structure, at least one of the dielectric layers functioning as a charge storage electrode for the memory device (paragraph [0138]); and

a control gate (218) formed over the plurality of dielectric layers (also paragraph [0138]).

As noted, a first insulating is not depicted in Figures 1 and 7. However, in paragraphs [0401] through [0412], particularly paragraph [0412], Lee describes at length how a buried oxide is formed on a standard silicon wafer substrate and teaches that the resulting structure, i.e., an insulating layer formed on a substrate, may be used in the pillar TFTs devices, i.e., the devices of Figures 1 through 9.

Referring to **claim 12**, Lee further discloses that the plurality of dielectric layers comprises:

a first oxide layer (704) formed around at least a portion of the conductive structure,

a nitride layer (706) formed around the first oxide layer, and

a second oxide layer (708) formed around the nitride layer, wherein the nitride layer acts as the charge storage electrode (paragraph [0138]).

Referring to **claim 13**, Lee further discloses that the conductive structure (206/208) is substantially cylindrical (Fig. 1B and paragraph [0125]) in shape and a first end (208) of the conductive structure acts as a drain region (paragraph [0126]) for the memory device.

5. **Claims 1-2, 4-5, and 16-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Hagemeyer U.S. Patent 6,768,166.

Hagemeyer discloses in Figures 1-10 and respective portions of the specification a memory device as claimed.

Referring to independent **claim 1**, Hagemeyer discloses a memory device, comprising:

a first conductive layer (201, Fig. 9), wherein a portion (103) of the first conductive layer acts as a source region (column 4, lines 30-35) for the memory device;

a conductive structure (104/109) formed on the first conductive layer, the conductive structure having a first end and a second end opposite the first end, wherein the first end is disposed adjacent the portion of the first conductive layer that acts as the source region for the memory device and wherein the second end acts as a drain region (109, column 4, lines 66-67) for the memory device;

a plurality of dielectric layers (105-107, Figs. 2 and 9) formed around at least a portion of the conductive structure, wherein at least one of the dielectric layers (106) acts as a floating gate electrode for the memory device (column 5, lines 9-11); and

a control gate (108, column 5, lines 7-9) formed over the plurality of dielectric layers.

Referring to independent **claim 16**, and using the same reference characters and citations as detailed above where applicable, Hagemeyer discloses a non-volatile memory array, comprising:

a first conductive layer (201, Fig. 9 and 1003, Fig. 10) formed on a substrate, wherein portions (103, fig. 9, not visible in Fig. 10) of the first conductive layer act as source regions for memory cells in the memory array;

a plurality of structures (104/109, Figs. 9 and 10) formed on the first conductive layer, wherein each of the plurality of structures functions as a channel region (column 4, lines 44-46) for one of the memory cells;

a plurality of dielectric layers formed around portions of each of the plurality of structures, wherein at least one of the plurality of dielectric layers functions as a charge storage electrode for one of the memory cells; and

at least one conductive layer (108) formed over the plurality of dielectric layers for each of the memory cells.

Referring to **claim 2**, Hagemeyer further discloses that the conductive structure (104/109, Figs. 1 and 2) is substantially cylindrical in shape.

Referring to **claim 4**, Hagemeyer further discloses an insulating layer (801 or the horizontal portion of oxide layer 105) formed on the first conductive layer (201) and adjacent the first end of the conductive structure.

Referring to **claims 5 and 17**, Hagemeyer further discloses that the plurality of dielectric layers comprises:

a first oxide layer (105) formed around the conductive structure,

a nitride layer (106) formed around the first oxide layer, and

a second oxide layer (107) formed around the nitride layer, wherein the nitride layer functions as the charge storage electrode or as the floating gate electrode (column 5, lines 9-11).

Referring to **claim 18**, Hagemeyer further discloses a plurality of bitlines (902 in Fig. 9, not shown in Fig. 10), wherein each of the plurality of bitlines contacts a number of the plurality of structures (104/109).

Referring to **claim 19**, Hagemeyer further discloses that the at least one conductive layer (108) comprises a plurality of conductive layers (108), wherein each of the conductive layers contacts a top one of the plurality of dielectric layers associated with a group of memory cells and functions as a word line (1002, column 7, lines 3035) for the non-volatile memory array.

Referring to **claim 20**, as noted above, Hagemeyer discloses that the plurality of structures (104/109) are each substantially cylindrical in shape and also as noted above a first end (109) of each of the plurality of structures functions as a drain region for one of the memory cells.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 3 and 6-8** are rejected under 35 U.S.C. §103(a) as being unpatentable over Hagemeyer for being obvious.

Referring to **claim 3**, Hagemeyer discloses a memory device as claimed and as detailed above including the conductive structure 104/109. However, the thickness of the conductive structure 104/109 is about no less than 1500 Å (150nm) instead of ranging from about 100 Å to about 1000 Å as claimed and a width of about 1500 Å (column 4, lines 48-52) instead of ranging from about 100 Å to about 1000 Å. Nevertheless, both Hagemeyer and Applicant have failed to disclose as to criticality of the differences of the sizes. Since the only difference between the prior art and the claims is a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the change in sizes would have been obvious at the time the invention was made and the claimed device is not patentably distinct from the prior art device.

Referring to **claims 6 and 7**, Hagemeyer discloses a memory device as claimed and as detailed above including the plurality of dielectric layers 105/106/107, which functions as a charge storage structure, comprising first oxide layer 105 (also known as tunneling gate oxide or simply as gate oxide in the art), the nitride layer 106 (also known as charge trapping layer or charge storage layer in the art or as described as "functioning as a floating gate electrode by Applicant), and the second oxide layer 107 (also known as intergate insulating layer in the art).

However, Hagemeyer is silent about the thickness of the layers. Nevertheless, the claimed thickness for the layers (each ranging from about 100 Å to about 500 Å in claim 6 and the combined thickness ranging from about 300 Å to about 1500 Å in claim 7), as will be detailed below, is known in the art. For example, Lai in U.S. Patent 6,551,880 discloses that thickness of the first dielectric is about 50 to 100 angstroms, the thickness of the silicon nitride is about 50 to 300 angstroms, and the thickness of the second silicon oxide is about 50 to 300 angstroms (Lai, column 3, lines 35-42). Since the only difference between the prior art and the claims is a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the change in sizes would have been obvious at the time the invention was made and the claimed device is not patentably distinct from the prior art device.

Referring to **claim 8**, similarly as explained above, since the only difference between the prior art and the claims is a recitation of relative dimensions of the control gate and a device having the claimed relative dimensions would not perform differently than the prior art device, the change in sizes would have been obvious at the time the invention was made and the claimed device is not patentably distinct from the prior art device.

7. **Claims 9-15** are rejected under 35 U.S.C. §103(a) as being unpatentable over Hagemeyer in view of Forbes U.S. Patent Application Publication 2003/0235075.

Referring to **claims 9-11**, Hagemeyer discloses a memory device as claimed and as detailed above including:

a substrate (101);

a conductive layer 201 over the substrate,

a conductive structure formed over the substrate, the conductive structure functioning as a channel region for the memory device;

a plurality of dielectric layers formed around at least a portion of the conductive structure, at least one of the dielectric layers functioning as a charge storage electrode for the memory device; and

a control gate formed over the plurality of dielectric layers.

However, Hagemeyer fails to disclose a first insulating layer formed on the substrate. In other words, Hagemeyer discloses a simple substrate of a single layer of silicon rather than a layered substrate having a substrate and a buried oxide layer on the substrate as claimed (SOI as is known in the art).

Forbes, in disclosing a memory device including first conductive layered layer 404/402 acting as a source region, a conductive structure 405 on the first conductive layered layer and having a first end disposed adjacent the first conductive layered layer and a second end acting as a drain region, an ONO layer 407 adjacent a sidewall of the conductive structure (in other words the Forbes' structure is substantially similar to Hagemeyer's and the claimed), teaches that the vertical channel memory device can be formed on a substrate such as a wafer and substrate including doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures (paragraph [0025]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the vertical channel structure of Hagemeyer including the claimed oxide layer. One would have been motivated to make such a modification in view of the

teachings in Forbes that vertical channel devices can be formed on a substrate including doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor substrate structures.

With respect to **claim 12**, Hagemeyer further discloses that the plurality of dielectric layers comprises:

a first oxide layer (105) formed around at least a portion of the conductive structure,

a nitride layer (106) formed around the first oxide layer, and

a second oxide layer (107) formed around the nitride layer, wherein the nitride layer acts as the charge storage electrode (column 5, lines 9-11).

Regarding **claim 13**, as mentioned above, Hagemeyer further discloses that the conductive structure is substantially cylindrical in shape and a first end of the conductive structure acts as a drain region for the memory device.

Referring to **claim 14**, as detailed above about the change in size for the plurality of dielectric layers, since the only difference between the prior art and the claims is a recitation of relative dimensions of the plurality of dielectric layers and a device having the claimed relative dimensions would not perform differently than the prior art device, the change in sizes would have been obvious at the time the invention was made and the claimed device is not patentably distinct from the prior art device.

Regarding **claim 15**, as mentioned above, Hagemeyer further discloses a second insulating layer formed on the first conductive layer and adjacent a lower portion of the conductive structure.

Conclusion

8 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,727,544 to Endoh et al. discloses a collection of transistors each having an ONO layer around a semiconductor island.

9 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
September 02, 2004